Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.040”**

**4 3**

**5**

**6**

**7**

**8**

**9**

**2**

**1**

**14**

**13**

**12**

**10 11**

**MASK**

**REF**

**74A**

**.040”**

**Top Material: Si**

**Backside Material: Al**

**Bond Pad Size: .0035” X .0035”**

**Backside Potential:**

**Mask Ref: 74A**

**APPROVED BY: DK DIE SIZE .040” X .040” DATE: 9/23/20**

**MFG: MOTOROLA THICKNESS .021” P/N: 54LS74**

**DG 10.1.2**

#### Rev B, 7/19/02